We Claim:

1. An integrated circuit, comprising:

a synchronous circuit;

an asynchronous circuit;

an input register circuit connected to said synchronous circuit and said asynchronous circuit, said input register circuit having a terminal receiving a first control clock signal for controlling data transfer;

an output register circuit connected to said synchronous circuit and said asynchronous circuit, said output register circuit having a terminal receiving a second control clock signal for controlling data transfer; and

a sequence controller;

said synchronous circuit storing data in said input register circuit so that the data can be processed in said asynchronous circuit;

said asynchronous circuit storing the processed data in said output register circuit so that the processed data can be further processed in said synchronous circuit; and

said sequence controller connected to said asynchronous circuit for generating the first control clock signal and the second control clock signal in dependence on a duration required for the data to be processed in said asynchronous circuit.

2. The integrated circuit according to claim 1, comprising:

a terminal for receiving a clock signal; and

a controllable switch switchably connecting together said terminal for receiving the clock signal and said terminal receiving the first control clock signal;

said controllable switch being controlled by said sequence controller.

3. The integrated circuit according to claim 2, wherein:

said terminal for receiving the clock signal is connected to said synchronous circuit and the clock signal controls operation of said synchronous circuit; and

the clock signal has a variably adjustable clock frequency.

4. The integrated circuit according to claim 1, wherein said sequence controller is contained in said asynchronous circuit.

5. The integrated circuit according to claim 1, wherein said asynchronous circuit includes a DRAM.

6. A method for operating the integrated circuit according to claim 1, the method which comprises:

activating said first control clock signal to transfer the data from said synchronous circuit into said input register circuit;

transferring the data from said input register circuit into said asynchronous circuit and processing the data in said asynchronous circuit to obtain the processed data;

with the sequence controller, inactivating the first control clock signal within the duration required for the data to be processed in said asynchronous circuit; and

not earlier than at a completion of the duration required for the data to be processed in said asynchronous circuit, using the second control clock signal to trigger transfer of the processed data into said output register circuit.

7. The method according to claim 6, which comprises:

providing a terminal for receiving a clock signal having an active state and an inactive state;

providing a controllable switch for switchably connecting together said terminal for receiving the clock signal and said terminal receiving the first control clock signal;

inactivating said first control clock signal by opening said controllable switch; and

using said sequence controller to close said controllable switch in the inactive state of the clock signal.